≡HT4818≡ / ≡HT4817≡

Dual 2.2W AUDIO AMPLIFIER Plus Stereo Headphone Function

General Description

The HT4818/7 is a dual bridge-connected audio power amplifier which, when connected to a 5V supply, will deliver 2.2W to a 4Ω load with less than 1.0% THD+N. In addition, the headphone input pin allows the amplifiers to operate in single-ended mode when driving stereo headphones.

Boomer audio power amplifiers were designed specifically to provide high quality output power from a surface mount package while requiring few external components. To simplify audio system design, the HT4818/7 combines dual bridge speaker amplifiers and stereo headphone amplifiers on one chip.

The HT4818/7 features an externally controlled, low-power consumption shutdown mode, a stereo headphone amplifier mode, and thermal shutdown protection. It also utilizes circuitry to reduce “clicks and pops” during device turn-on.

Key Specifications

- P_O at 1% THD+N
  4Ω loads 2.2W(typ), 8Ω load 1.1W(typ)
- Single-ended mode THD+N at 75mW into 32Ω 0.5%(max)
- Shutdown current 0.7μA(typ)
- Supply voltage range 2.5 V to 5.5V

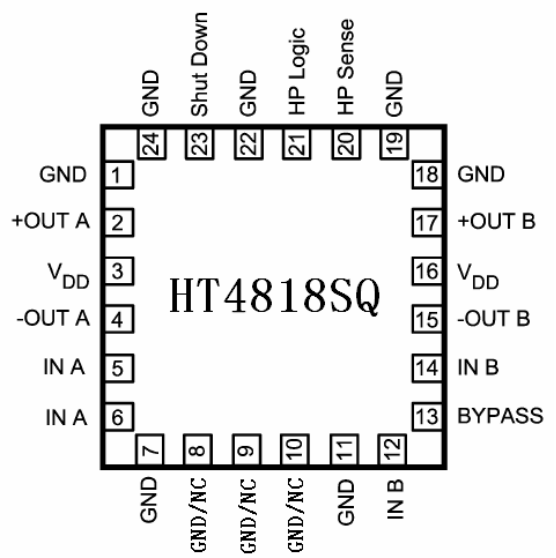
Features

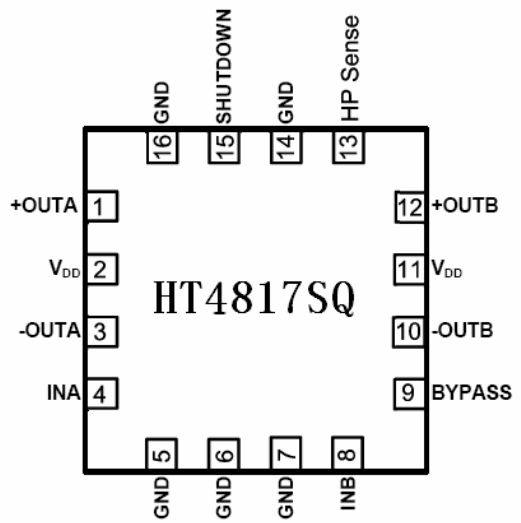
- Stereo headphone amplifier mode
- “Click and pop” suppression circuitry
- Unity-gain stable
- Thermal shutdown protection circuitry
- QFN24/QFN16 packages

Applications

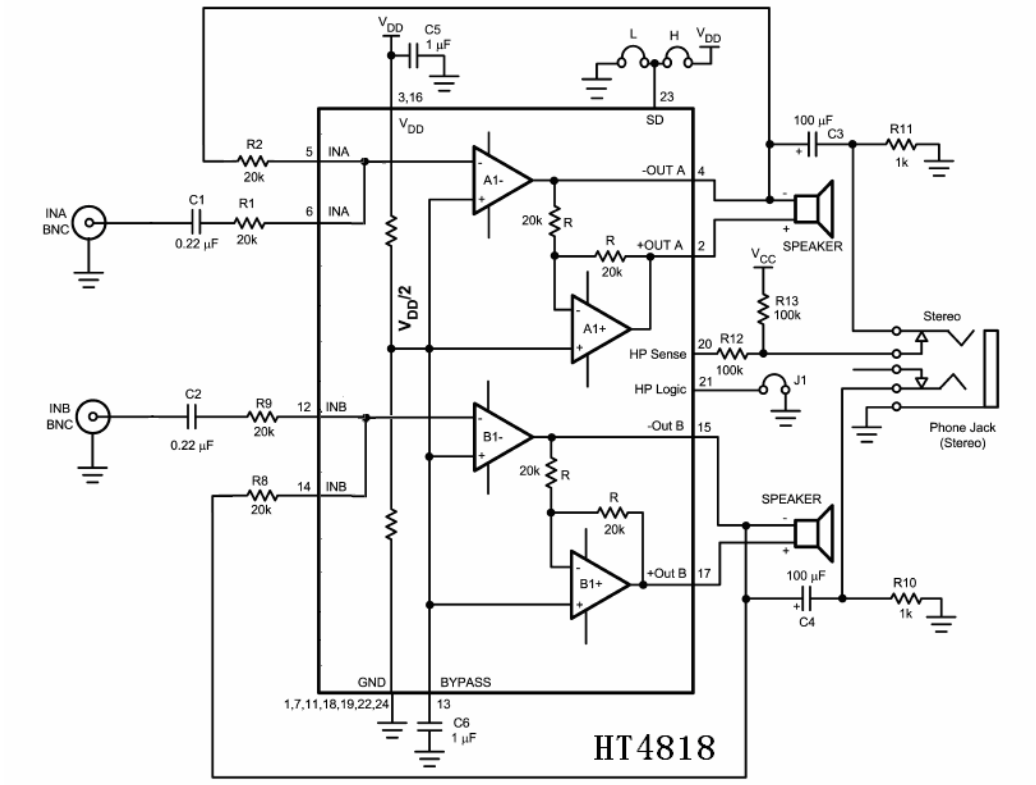
- Cell phones
- Multimedia monitors
- Portable and desktop computers
- Portable audio systems

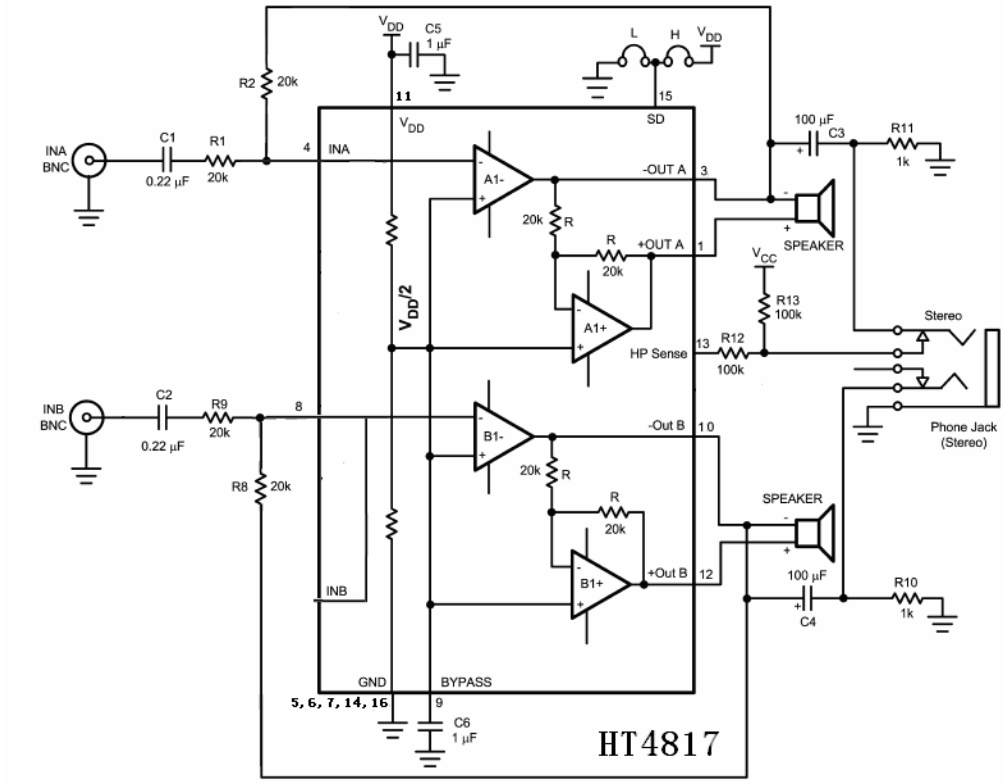
Connection Diagrams





Typical Application





Absolute Maximum Ratings

Supply Voltage	6.0V	Solder Information	
Storage Temperature	−65°C to +150°C	Small Outline Package	
Input Voltage	−0.3V to V_{DD}+0.3V	Vapor Phase (60 sec.)	215°C
Power Dissipation	Internally limited	Infrared (15 sec.)	220°C
ESD Susceptibility	2000V	Thermal Resistance	
ESD Susceptibility	200V	θ_{JC} (typ)—SQA24B	3°C/W
Junction Temperature	150°C	θ_{JA} (typ)—SQA24B	42°C/W

Operating Ratings

Temperature Range

$T_{MIN} \leqslant T_A \leqslant T_{MAX}$	−40°C $\leqslant T_A \leqslant$ 85°C
Supply Voltage	2.7V $\leqslant V_{DD} \leqslant$ 5.5V

Electrical Characteristics (5V)

The following specifications apply for V_{DD} = 5V unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	HT4818		Units (Limits)
			Typical	Limit	
V_{DD}	Supply Voltage			2.7	V (min)
				5.5	V (max)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A , BTL mode	6	10	mA (max)
		V_{IN} = 0V, I_O = 0A , SE mode	3.0	6	mA (max)
I_{SD}	Shutdown Current	GND applied to the SHUTDOWN pin	0.04	2	µA (max)
V_{IH}	Headphone Sense High Input Voltage		3.7	4	V (min)
V_{IL}	Headphone Sense Low Input Voltage		2.6	0.8	V (max)
V_{IHSD}	Shutdown, Headphone micro, High Input voltage		1.2	1.4	V (min)
V_{ILSD}	Shutdown, Headphone micro, Low Input voltage		1	0.4	V (max)
T_{WU}	Turn On Time	1µF Bypass Cap (C6)	140		ms

Electrical Characteristics for Single-Ended Operation (5V)

The following specifications apply for V_{DD} = 5V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	HT4818		Units (Limits)
			Typical	Limit	
P_O	Output Power	THD+N = 0.5%, f = 1 kHz, R_L = 32Ω	90	75	mW (min)
THD+N	Total Harmonic Distortion+Noise	P_O = 20mW, 1kHz, R_L = 32Ω	0.015		%
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	70		dB
		Input Unterminated, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	72		dB
		Input grounded, 217Hz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	65		dB
		Input grounded, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	70		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1.0µF	80		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	11		µV

Electrical Characteristics for Bridged-Mode Operation (5V)

The following specifications apply for V_{DD} = 5V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	HT4818		Units (Limits)
			Typical	Limit	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5	25	mV (max)
P_O	Output Power	THD+N = 1%, f = 1kHz			
		HT4818SQ , R_L = 3Ω	2.5		W
		HT4818SQ , R_L = 4Ω	2.2		W
		HT4818SQ, R_L = 8Ω	1.3	1.0	W (min)
		THD+N = 10%, f = 1kHz			
		HT4818SQ , R_L = 3Ω	3.0		W
		HT4818SQ , R_L = 4Ω	2.5		W
		HT4818SQ , R_L = 8Ω	1.7		W
THD+N	Total Harmonic Distortion+Noise	1kHz, A_{VD} = 2			
		HT4818SQ , R_L = 4Ω, P_O = 1W	0.10		%
		HT4818SQ , R_L = 8Ω, P_O = .4W	0.06		%
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple} = 200mV_{p-p} C_6 = 1µF, R_L = 8Ω	85		dB
		Input Unterminated, 1kHz V_{ripple} = 200mV_{p-p} C_6 = 1µF, R_L = 8Ω	80		dB
		Input grounded, 217Hz V_{ripple} = 200mV_{p-p} C_6 = 1µF, R_L = 8Ω	65		dB
		Input grounded, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 8Ω	70		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1.0µF	82		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	21		µV

Electrical Characteristics (3V)

The following specifications apply for V_{DD} = 3V unless otherwise noted. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	HT4818		Units (Limits)
			Typical	Limit	
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, I_O = 0A , BTL mode	4.5		mA
		V_{IN} = 0V, I_O = 0A , SE mode	2.5		mA
I_{SD}	Shutdown Current	GND applied to the SHUTDOWN pin	0.01		µA
V_{IH}	Headphone High Input Voltage		2.2		V
V_{IL}	Headphone Low Input Voltage		1.5		V
V_{IHSD}	Shutdown, Headphone micro, High Input voltage		1	1.4	V (min)
V_{ILSD}	Shutdown, Headphone micro, Low Input voltage		0.8	.4	V (max)
T_{WU}	Turn On Time	1µF Bypass Cap (C6)	140		ms

Electrical Characteristics for Bridged-Mode Operation (3V)

The following specifications apply for V_{DD} = 3V unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	HT4818		Units (Limits)
			Typical	Limit	
V_{OS}	Output Offset Voltage	V_{IN} = 0V	5		mV
P_O	Output Power	THD+N = 1%, f = 1kHz			
		HT4818SQ, R_L = 3Ω	.82		W
		HT4818SQ, R_L = 4Ω	.70		W
		HT4818SQ, R_L = 8Ω	.43		W
		THD+N = 10%, f = 1kHz			
		HT4818SQ, R_L = 3Ω	1.0		W
		HT4818SQ, R_L = 4Ω	.85		W
		HT4818SQ, R_L = 8Ω	.53		W
THD+N	Total Harmonic Distortion+Noise	1kHz			
		HT4818SQ, R_L = 4Ω, P_O = 280mW	0.1		%
		HT4818SQ, R_L = 8Ω, P_O = 200mW	0.05		%
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 8Ω	90		dB
		Input Unterminated, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 8Ω	80		dB
		Input grounded, 217Hz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 8Ω	65		dB
		Input grounded, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 8Ω	73		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1.0µF	85		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	21		µV

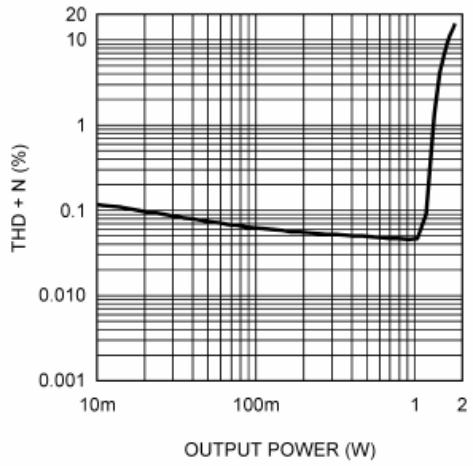
Electrical Characteristics for Single-Ended Operation (3V)

The following specifications apply for V_{DD} = 3V unless otherwise specified. Limits apply for T_A = 25°C.

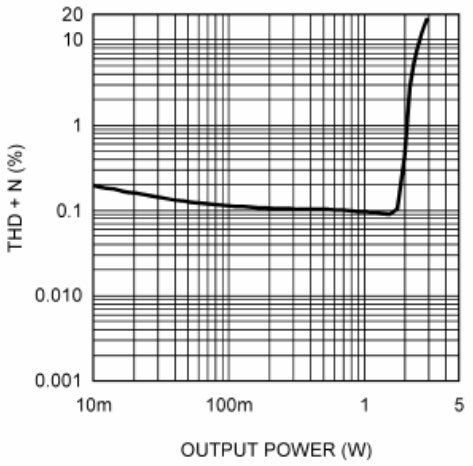
Symbol	Parameter	Conditions	HT4818		Units (Limits)
			Typical	Limit	
P_O	Output Power	THD+N = 0.5%, f = 1 kHz, R_L = 32Ω	35		mW
THD+N	Total Harmonic Distortion+Noise	P_O = 25mW, 1kHz, R_L = 32Ω	.015		%
PSRR	Power Supply Rejection Ratio	Input Unterminated, 217Hz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	71		dB
		Input Unterminated, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	79		dB
		Input grounded, 217Hz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	65		dB
		Input grounded, 1kHz V_{ripple} = 200mV_{p-p} C_6= 1µF, R_L = 32Ω	72		dB
X_{TALK}	Channel Separation	f = 1kHz, C_6 = 1.0µF	80		dB
V_{NO}	Output Noise Voltage	1kHz, A-weighted	11		µV

Typical Performance Characteristics

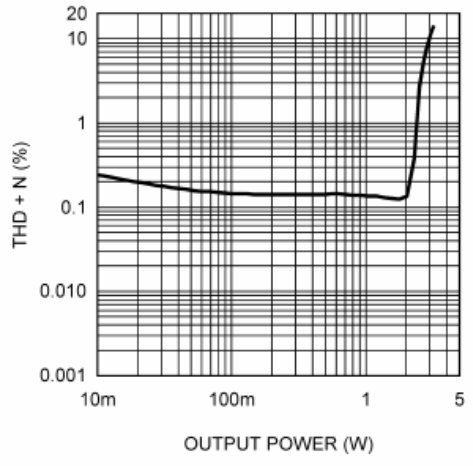
THD+N vs Output Power
5V, 8Ω, BTL at 1kHz



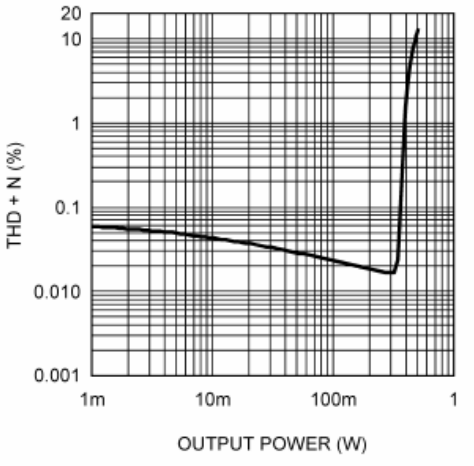
THD+N vs Output Power
5V, 4Ω, BTL at 1kHz



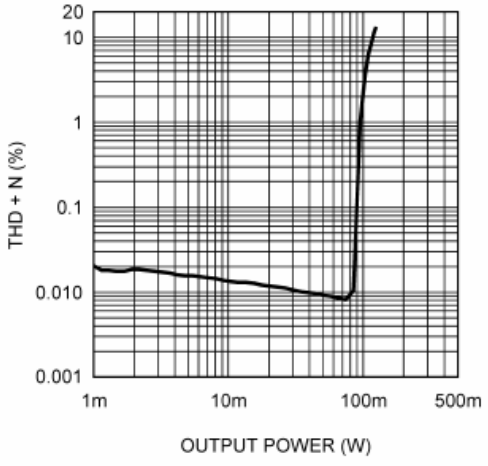
THD+N vs Output Power
5V, 3Ω, BTL at 1kHz



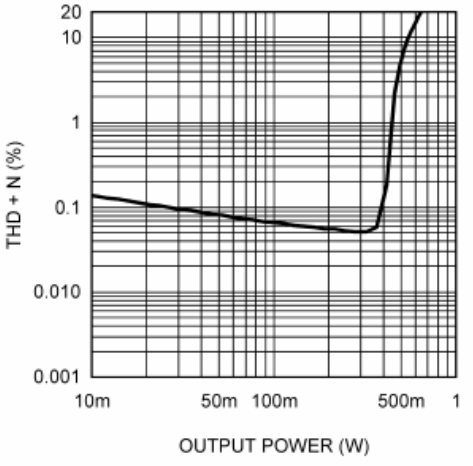
THD+N vs Output Power
5V, 32Ω, BTL at 1kHz



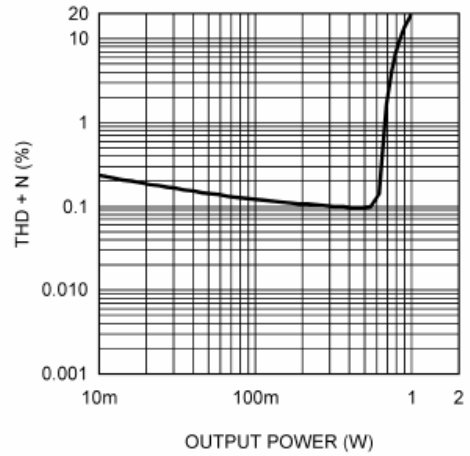
THD+N vs Output Power
5V, 32Ω, SE at 1kHz



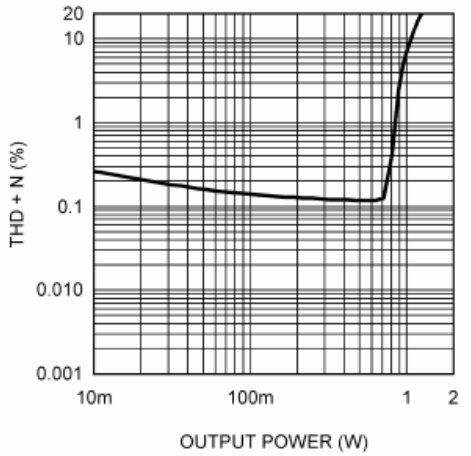
THD+N vs Output Power
3V, 8Ω, BTL at 1kHz



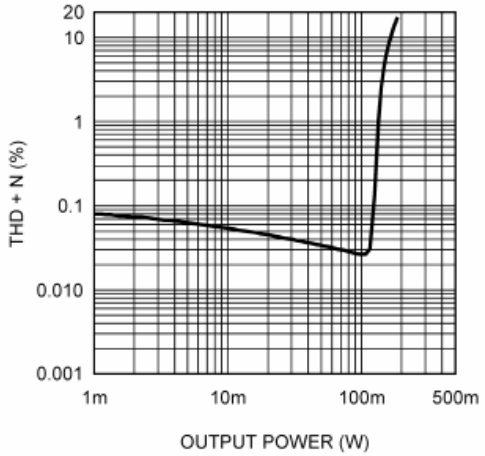
THD+N vs Output Power
3V, 4Ω, BTL at 1kHz



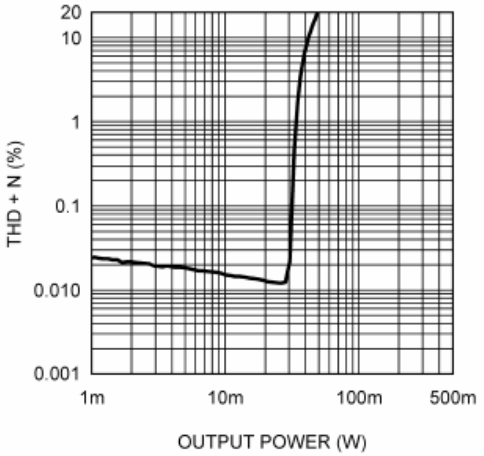
THD+N vs Output Power
3V, 3Ω, BTL at 1kHz



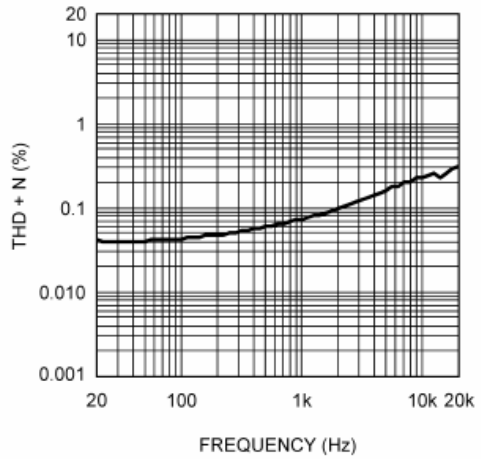
THD+N vs Output Power
3V, 32Ω, BTL at 1kHz



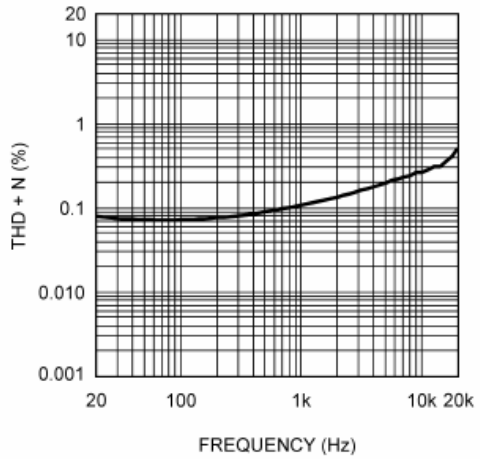
THD+N vs Output Power
3V, 32Ω, SE at 1kHz



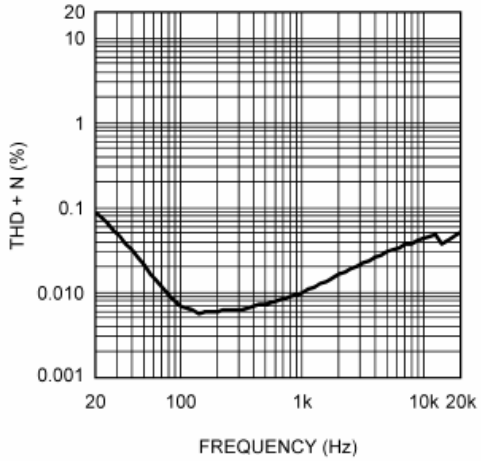
THD+N vs Frequency
5V, 8Ω, BTL at 400mW



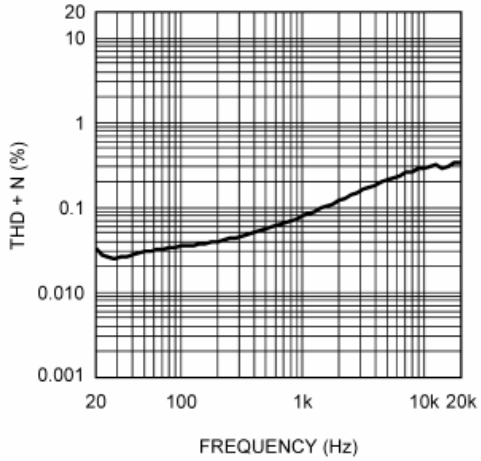
THD+N vs Frequency
5V, 4Ω, BTL at 1W



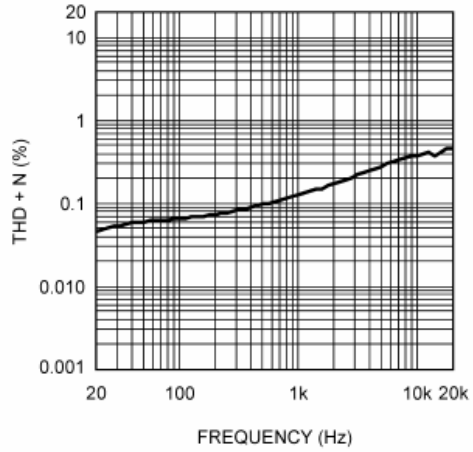
THD+N vs Frequency
5V, 32Ω, SE at 75mW



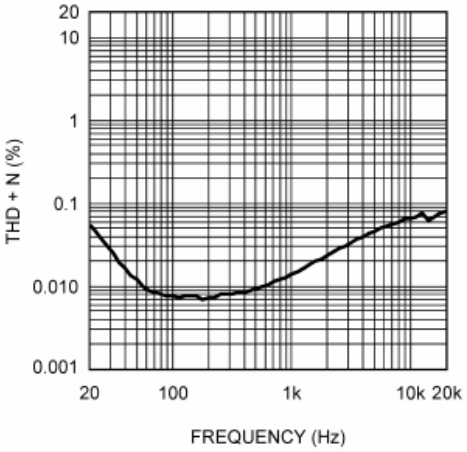
THD+N vs Frequency
3V, 8Ω, BTL at 150mW



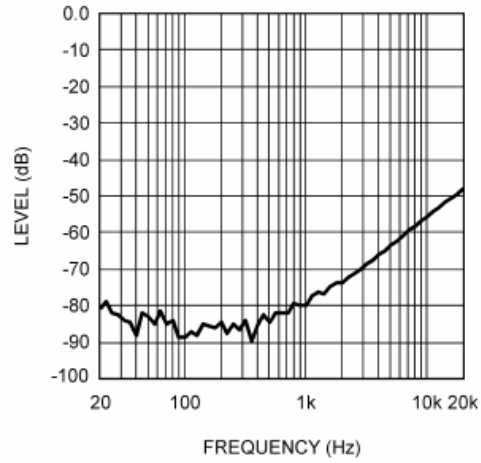
THD+N vs Frequency
3V, 4Ω, BTL at 250mW



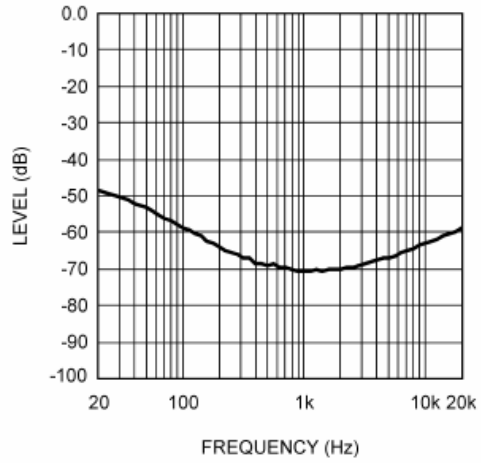
THD+N vs Frequency
3V, 32Ω, SE at 25mW



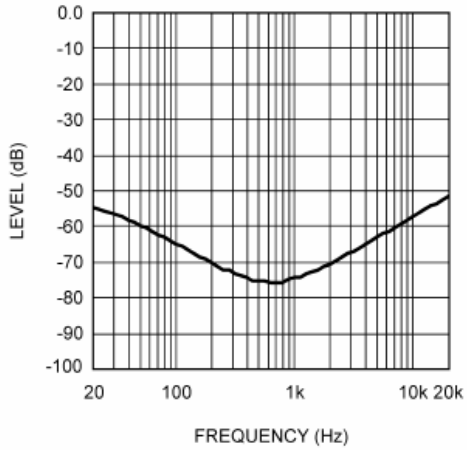
PSRR
5V, 8Ω, BTL, Input Unterminated



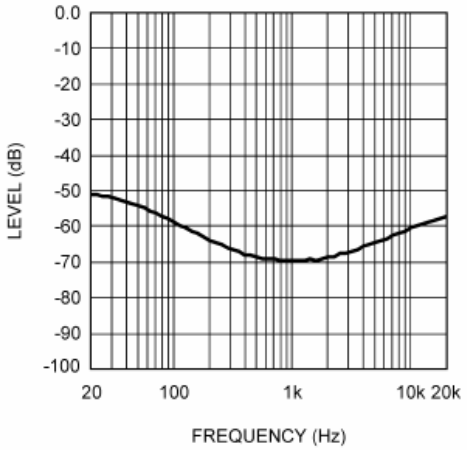
PSRR
5V, 8Ω, BTL, Input Terminated



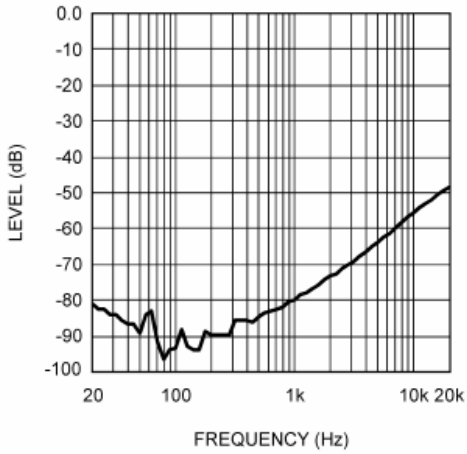
PSRR
5V, 32Ω, SE, Input Unterminated



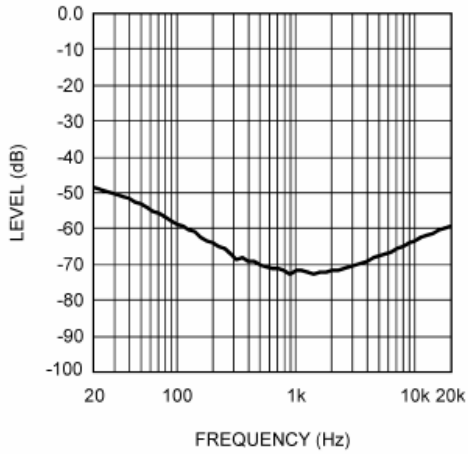
PSRR
5V, 32Ω, SE, Input Terminated



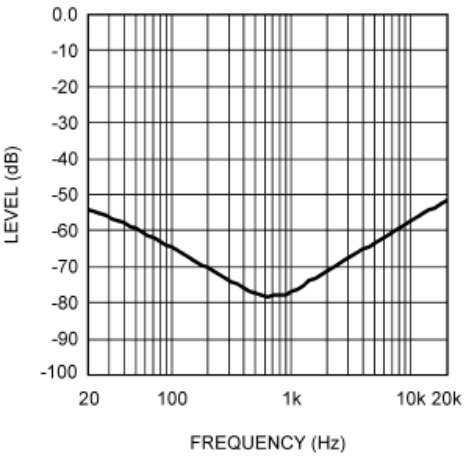
PSRR
3V, 8Ω, BTL, Input Unterminated



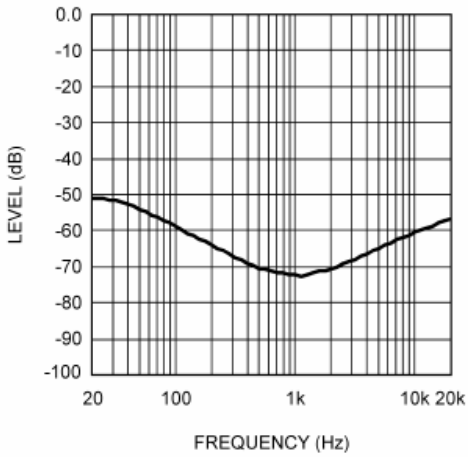
PSRR
3V, 8Ω, BTL, Input Terminated



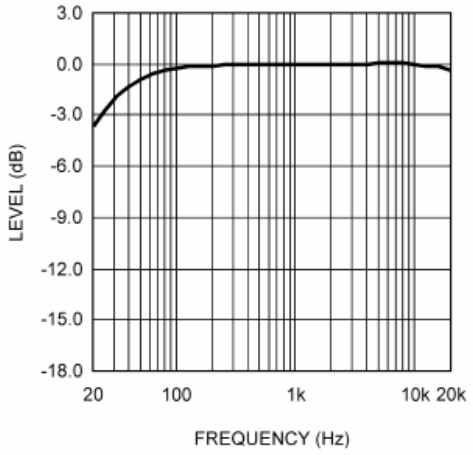
PSRR
3V, 32Ω, SE, Input Unterminated



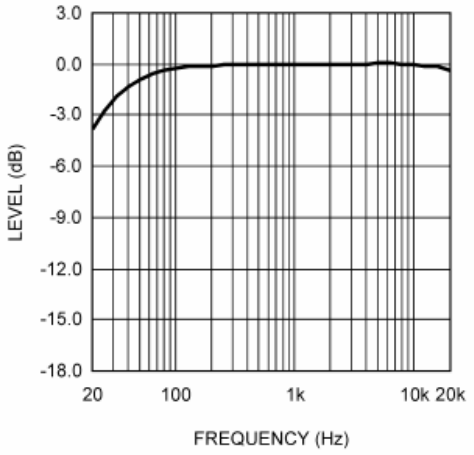
PSRR
3V, 32Ω, SE, Input Terminated



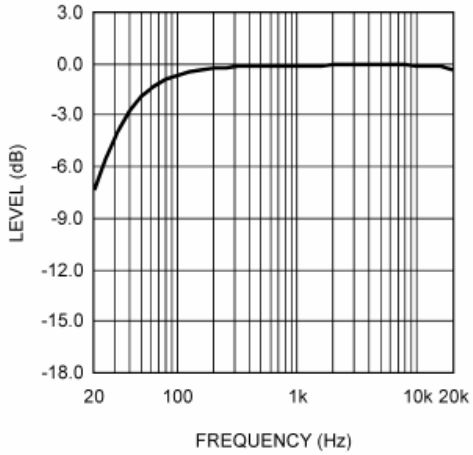
Frequency Response
5V, 8Ω, BTL



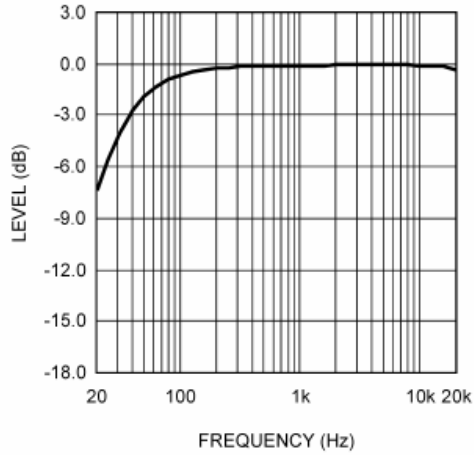
Frequency Response
3V, 8Ω, BTL



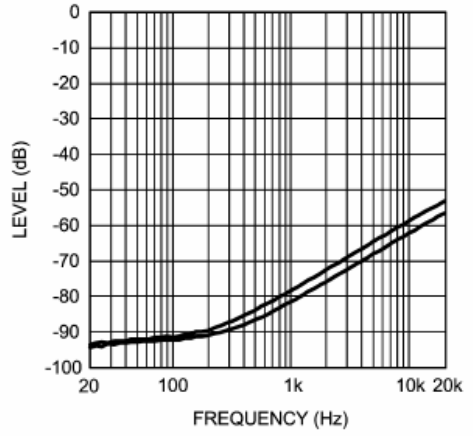
Frequency Response
5V, 32Ω, SE



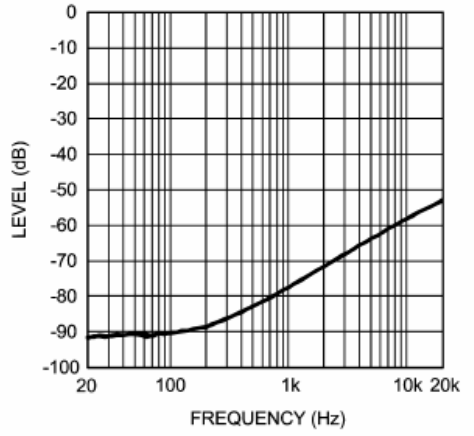
Frequency Response
3V, 32Ω, SE



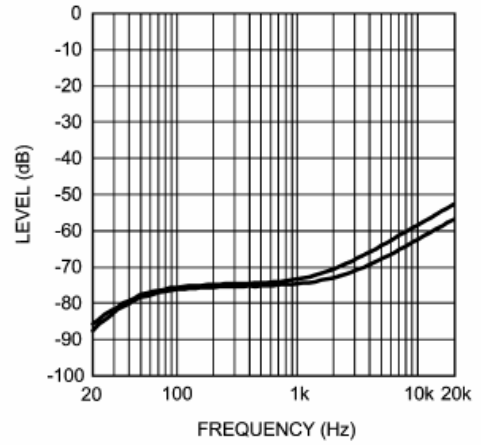
Crosstalk
5V, 8Ω, BTL



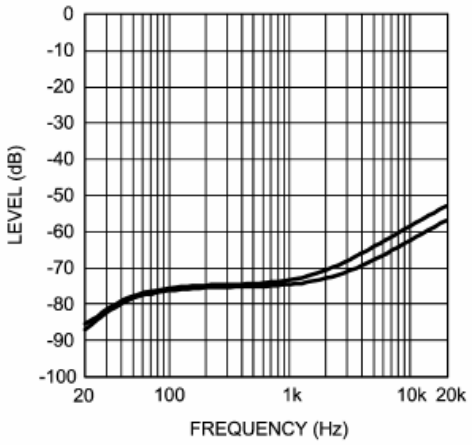
Crosstalk
3V, 8Ω, BTL



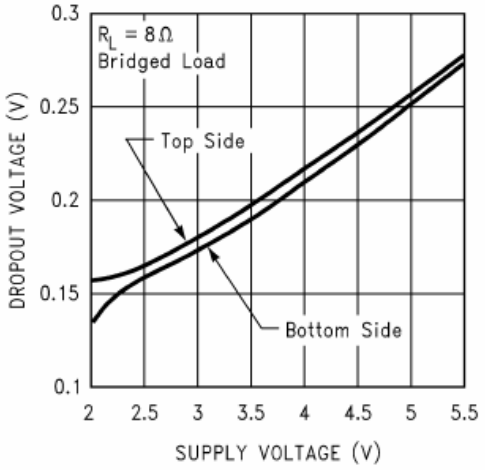
Crosstalk
3V, 32Ω, SE



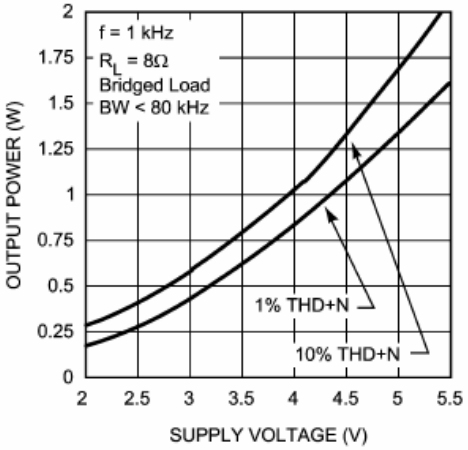
Crosstalk
5V, 32Ω, SE



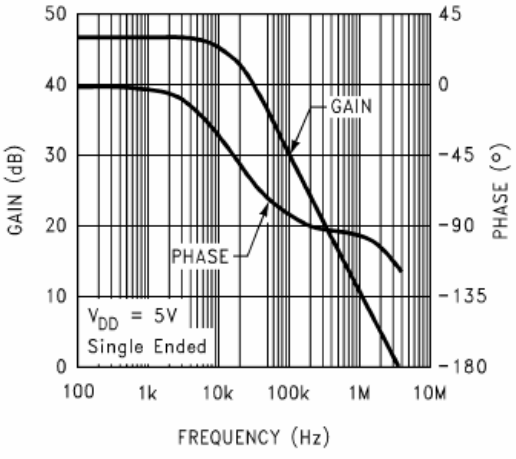
Dropout Voltage vs
Supply Voltage



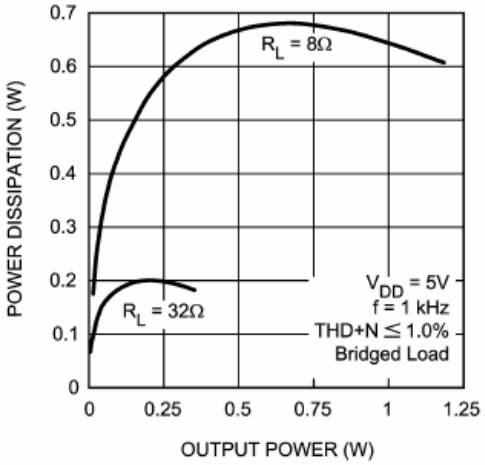
Output Power vs
Supply Voltage

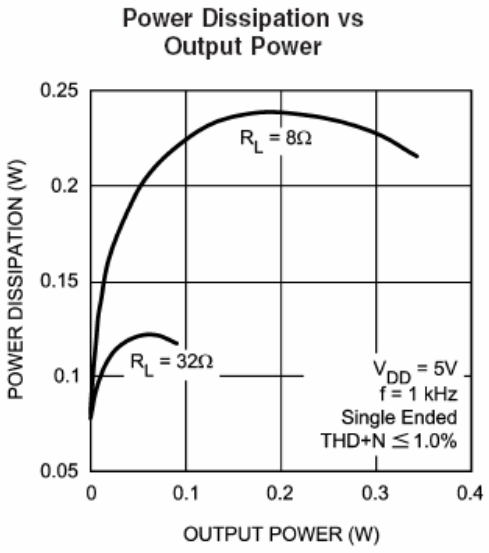


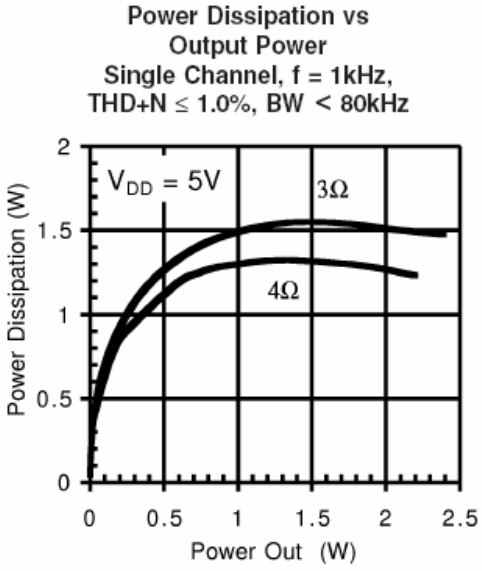
Open Loop
Frequency Response

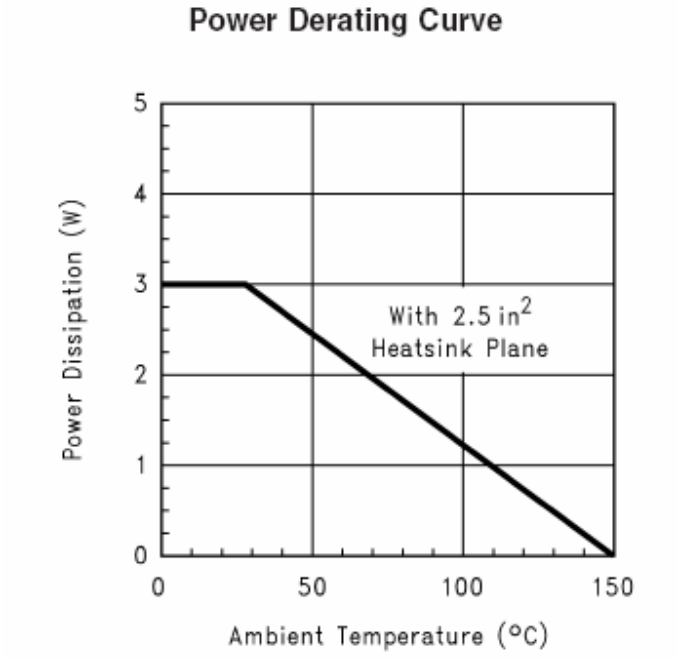


Power Dissipation vs
Output Power









Application Information

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATIONS

The HT4818/7's SQ exposed-DAP (die attach paddle) package provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane and, finally, surrounding air. The result is a low voltage audio power amplifier that produces 2.1W at 0.1% THD with a 4 Ω load. This high power is achieved through careful consideration of necessary thermal design. Failing to optimize thermal design may compromise the HT4818/7's high power performance and activate unwanted, though necessary, thermal shutdown protection. The SQ package must have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad is connected to a large plane of continuous unbroken copper. This plane forms a thermal mass and heat sink and radiation area. Place the heat sink area on either outside plane in the case of a two-sided PCB, or on an inner layer of a board with more than two layers. Connect the DAP copper pad to the inner layer or backside copper heat sink area with 6 (3x2) SQ vias. The via diameter should be 0.012in–0.013in with a 1.27mm pitch. Ensure efficient thermal conductivity by platingthrough and solder-filling the vias.

Best thermal performance is achieved with the largest practical copper heat sink area. If the heatsink and amplifier share the same PCB layer, a nominal 2.5in^2 (min) area is necessary for 5V operation with a 4 Ω load. Heatsink areas not placed on the same PCB layer as the HT4818/7 should be 5in^2 (min) for the same supply voltage and load resistance. The last two area recommendations apply for 25°C ambient temperature. Increase the area to compensate

for ambient temperatures above 25°C. In all circumstances and conditions, the junction temperature must be held below 150°C to prevent activating the HT4818/7's thermal shutdown protection. The HT4818/7's power de-rating curve in the **Typical Performance Characteristics** shows the maximum power dissipation versus temperature. Example PCB layouts for the exposed-Dap SQ package is shown in the **Demonstration Board Layout** section.

PCB LAYOUT AND SUPPLY REGULATION
CONSIDERATIONS FOR DRIVING 3Ω AND 4Ω LOADS

Power dissipated by a load is a function of the voltage swing across the load and the load's impedance. As load impedance decreases, load dissipation becomes increasingly dependent on the interconnect (PCB trace and wire) resistance between the amplifier output pins and the load's connections. Residual trace resistance causes a voltage drop, which results in power dissipated in the trace and not in the load as desired. For example, 0.1Ω trace resistance reduces the output power dissipated by a 4Ω load from 2.1W to 2.0W. This problem of decreased load dissipation is exacerbated as load impedance decreases. Therefore, to maintain the highest load dissipation and widest output voltage swing, PCB traces that connect the output pins to a load must be as wide as possible.

Poor power supply regulation adversely affects maximum output power. A poorly regulated supply's output voltage decreases with increasing load current. Reduced supply voltage causes decreased headroom, output signal clipping, and reduced output power. Even with tightly regulated supplies, trace resistance creates the same effects as poor supply regulation. Therefore, making the power supply traces as wide as possible helps maintain full output voltage swing.

BRIDGE CONFIGURATION EXPLANATION

As shown in Figure 1, the HT4818/7 consists of two pairs of operational amplifiers, forming a two-channel (channel A and channel B) stereo amplifier. External feedback resistors R2 (or R3, R4) and R8 (or R6, R7) and input resistors R1 and R9 set the closed-loop gain of Amp A (-out) and Amp B (-out) whereas two internal 20kΩ resistors set Amp A's (+out) and Amp B's (+out) gain at 1. The HT4818/7 drives a load, such as a speaker, connected between the two amplifier outputs, −OUTA and +OUTA.

Figure 1 shows that Amp A's (-out) output serves as Amp A's (+out) input. This results in both amplifiers producing signals identical in magnitude, but 180° out of phase. Taking advantage of this phase difference, a load is placed between −OUTA and +OUTA and driven differentially (commonly referred to as "bridge mode"). This results in a differential gain of

$$A_{VD} = 2 * (R_f / R_i) \quad (1)$$

or

$$A_{VD} = 2 * (R_2 / R_1)$$

Bridge mode amplifiers are different from single-ended amplifiers that drive loads connected between a single amplifier's output and ground. For a given supply voltage, bridge mode has a distinct advantage over the single-ended configuration: its differential output doubles the voltage swing across the load. This produces four times the output power when compared to a single-ended amplifier under the same conditions. This increase in attainable output power assumes that the amplifier is not current limited or that the output signal is not clipped. To ensure minimum output signal clipping when choosing an amplifier's closed-loop gain, refer to the **Audio Power Amplifier Design** section.

Another advantage of the differential bridge output is no net DC voltage across the load. This is accomplished by biasing channel A's and channel B's outputs at half-supply. This eliminates the coupling capacitor that single supply, singleended amplifiers require. Eliminating an output coupling capacitor in a single-ended configuration forces a single-supply amplifier's half-supply bias voltage across the load. This increases internal IC power dissipation and may permanently damage loads such as speakers.

POWER DISSIPATION

Power dissipation is a major concern when designing a successful single-ended or bridged amplifier. Equation (2) states the maximum power dissipation point for a singleended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{DMAX} = (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Single-Ended} \quad (2)$$

However, a direct consequence of the increased power delivered to the load by a bridge amplifier is higher internal power dissipation for the same conditions.

The HT4818/7 has two operational amplifiers per channel. The maximum internal power dissipation per channel operating in the bridge mode is four times that of a single-ended amplifier. From Equation (3), assuming a 5V power supply and a 4Ω load, the maximum single channel power dissipation is 1.27W or 2.54W for stereo operation.

$$P_{DMAX} = 4 * (V_{DD})^2 / (2\pi^2 R_L) \quad \text{Bridge Mode} \quad (3)$$

The HT4818/7's power dissipation is twice that given by Equation (2) or Equation (3) when operating in the single-ended mode or bridge mode, respectively. Twice the maximum power dissipation point given by Equation (3) must not exceed the power dissipation given by Equation (4):

$$P_{DMAX}' = (T_{JMAX} - T_A) / \theta_{JA} \quad (4)$$

The HT4818/7's T_{JMAX} = 150°C. In the SQ package soldered to a DAP pad that expands to a copper area of 5in^2 on a PCB, the HT4818/7's θ_{JA} is 20°C/W. At any given ambient temperature T_A, use Equation (4) to find the maximum internal power dissipation supported by the IC packaging. Rearranging Equation (4) and substituting P_{DMAX} for P_{DMAX}' results in Equation (5). This equation gives the maximum ambient temperature that still allows maximum stereo power dissipation without violating the HT4818/7's maximum junction temperature.

$$T_A = T_{JMAX} - 2*P_{DMAX}\theta_{JA} \quad (5)$$

For a typical application with a 5V power supply and an 4Ω load, the maximum ambient temperature that allows maximum stereo power dissipation without exceeding the maximum junction temperature is approximately 99°C for the SQ package.

$$T_{JMAX} = P_{DMAX}\theta_{JA} + T_A \quad (6)$$

Equation (6) gives the maximum junction temperature T_{JMAX}. If the result violates the HT4818/7's 150°C, reduce the maximum junction temperature by reducing the power supply voltage or increasing the load resistance. Further allowance should be made for increased ambient temperatures. The above examples assume that a device is a surface mount part operating around the maximum power dissipation point. Since internal power dissipation is a function of output power, higher ambient temperatures are allowed as output power or duty cycle decreases.

If the result of Equation (2) is greater than that of Equation (3), then decrease the supply voltage, increase the load impedance, or reduce the ambient temperature. If these measures are insufficient, a heat sink can be added to reduce θ_{JA}. The heat sink can be created using additional copper area around the package, with connections to the ground pin(s), supply pin and amplifier output pins. External, solder attached SMT heatsinks such as the Thermalloy 7106D can also improve power dissipation. When adding a heat sink, the θ_{JA} is the sum of θ_{JC}, θ_{CS}, and θ_{SA}. (θ_{JC} is the junction-to-case thermal impedance, θ_{CS} is the case-to-sink thermal impedance, and θ_{SA} is the sink-to-ambient thermal impedance.) Refer to the **Typical Performance Characteristics** curves for power dissipation information at lower output power levels.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10 µF in parallel with a 0.1 µF filter capacitor to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 1.0 µF tantalum bypass capacitance connected between the HT4818/7's supply pins and ground. Do not substitute a ceramic capacitor for the tantalum. Doing so may cause oscillation. Keep the length of leads and traces that connect capacitors between the HT4818/7's power supply pin and ground as short as possible.

MICRO-POWER SHUTDOWN

The voltage applied to the SHUTDOWN pin controls the HT4818/7's shutdown function. Activate micro-power shutdown by applying GND to the SHUTDOWN pin. When active, the HT4818/7's micro-power shutdown feature turns off the amplifier's bias circuitry, reducing the supply current. The low 0.04 µA typical shutdown current is achieved by applying a voltage that is as near as GND as possible to the SHUTDOWN pin. A voltage that is more than GND may increase the shutdown current. *Table 1* shows the logic signal levels that activate and deactivate micro-power shutdown and headphone amplifier operation.

There are a few ways to control the micro-power shutdown. These include using a single-pole, single-throw switch, a microprocessor, or a microcontroller. When using a switch, connect an external 100k resistor between the SHUTDOWN pin and Ground. Connect the switch between the SHUTDOWN pin V_{DD}. Select normal amplifier operation by closing the switch. Opening the switch sets the SHUTDOWN pin to ground through the 100k resistor, which activates the micropower shutdown. The switch and resistor guarantee that the SHUTDOWN pin will not float. This prevents unwanted state changes. In a system with a microprocessor or a microcontroller, use a digital output to apply the control voltage to the SHUTDOWN pin. Driving the SHUTDOWN pin with active circuitry eliminates the pull up resistor.

TABLE 1. Logic Level Truth Table

SHUTDOWN PIN	HEADPHONE LOGIC PIN	HEADPHONE JACK SENSE PIN	OPERATIONAL OUTPUT MODE
Logic High	High	Don't Care	SINGLE ENDED
Logic High	Low	Low (HP not plugged in)	BRIDGED/BTL
Logic High	Don't Care	High (HP plugged in)	SINGLE ENDED
Logic Low	Don't Care	Don't Care	Micro-Power Shutdown

HEADPHONE SENSE AND HEADPHONE LOGIC IN FUNCTIONS

Applying a logic level to the HT4818/7's HP Sense headphone control pin turns off Amp A (+out) and Amp B (+out) muting a bridged-connected load. Quiescent current consumption is reduced when the IC is in this single-ended mode.

Figure 2 shows the implementation of the HT4818/7's headphone control function. With no headphones connected to the headphone jack, the R11-R13 voltage divider sets the voltage applied to the HP Sense pin (pin 20) at approximately 50mV. This 50mV enables Amp A (+out) and Amp B (+out) placing the HT4818/7 in bridged mode operation.

While the HT4818/7 operates in bridged mode, the DC potential across the load is essentially 0V. Therefore, even in an ideal situation, the output swing cannot cause a false singleended trigger. Connecting headphones to the headphone jack disconnects the headphone jack contact pin from −OUTA and allows R13 to pull the HP Sense pin up to V_{DD}. This enables the headphone function, turns off Amp A (+out) and Amp B (+out) which mutes the bridged speaker. The amplifier then drives the headphones, whose impedance is in parallel with resistors R10 and R11. These resistors have negligible effect on the HT4818/7's output drive capability since the typical impedance of headphones is 32∧.

Figure 2 also shows the suggested headphone jack electrical connections. The jack is designed to mate with a threewire plug. The plug's tip and ring should each carry one of the two stereo output signals, whereas the sleeve should carry the ground return. A headphone jack with one control pin contact is sufficient to drive the HP Sense pin when connecting headphones.

There is also a second input circuit that can control the choice of either BTL or SE modes. This input control pin is called the HP (Headphone) Logic Input. When the HP Logic input is high, HT4818/7 operates in SE mode. When HP Logic is low (& the HP Sense pin is low), the HT4818/7 operates in the BTL mode. In the BTL mode (HP Logic low and HP Sense Low) if the Headphones are connected directly to the Single Ended outputs (not using the HP Sense pin on the HP Jack) then both the Speaker (BTL) and Headphone (SE) will be functional. In this case the inverted op amp outputs drive the Speaker as well as the HP load, i.e. 8 ohms in parallel with 32 ohms. As the HT4818/7 is capable of driving up to a 3 ohm load driving the Speakers and the Headphones at the same time will not be a problem as long as the parallel resistance of each Speaker and each Headphone driver are more than 3 ohms.

As outlined above driving the Speaker (BTL) and Headphone (SE) loads simultaneously using HT4818/7 is simple and easy. However this configuration will only work if the HP Logic pin is used to control the BTL/SE operation and HP Sense pin is connected to GND.

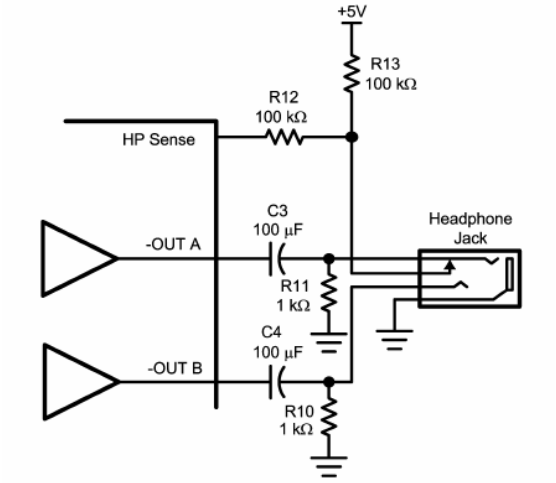


FIGURE 2. Headphone Circuit

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the HT4818/7's performance requires properly selecting external components. Though the HT4818/7 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values. The HT4818/7 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the **Audio Power Amplifier Design** section for more information on selecting the proper gain.

Input Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input coupling capacitors (C1 and C2) in Figure 1. A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150 Hz. Applications using speakers with this limited frequency response reap little improvement by using large input capacitor.

Besides effecting system cost and size, C1 and C2 have an effect on the HT4818/7's click and pop performance. When the supply voltage is first applied, a transient (pop) is created as the charge on the input capacitor changes from zero to

a quiescent state. The magnitude of the pop is directly proportional to the input capacitor's size. Higher value capacitors need more time to reach a quiescent DC voltage (usually $V_{DD}/2$) when charged with a fixed current. The amplifier's output charges the input capacitor through the feedback resistors, R2 and R8. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired −3dB frequency.

A shown in Figure 1, the input resistors (R1,4,5, and 6) and the input capacitors, C1 and C2 produce a −3dB high pass filter cutoff frequency that is found using Equation (7). (7) As an example when using a speaker with a low frequency limit of 150Hz, C_1, using Equation (7) is 0.053µF. The .33µF C_1 shown in Figure 1 allows the HT4818/7 to drive high efficiency, full range speaker whose response extends below 30Hz.

Bypass Capacitor Value Selection

Besides minimizing the input capacitor size, careful consideration should be paid to value of C_6, the capacitor connected to the BYPASS pin. Since C_6 determines how fast the HT4818/7 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the HT4818/7's outputs ramp to their quiescent DC voltage (nominally 1/2 V_{DD}), the smaller the turn-on pop. Choosing C_6 equal to 1.0 µF along with a small value of C_1 (in the range of 0.1 µF to 0.39 µF), produces a click-less and pop-less shutdown function. As discussed above, choosing C_1 no larger than necessary for the desired bandwith helps minimize clicks and pops. Connecting a 1µF capacitor, C_6, between the BYPASS pin and ground improves the internal bias voltage's stability and improves the amplifier's PSRR.

OPTIMIZING CLICK AND POP REDUCTION PERFORMANCE

The HT4818/7 contains circuitry that minimizes turn-on and shutdown transients or "clicks and pop". For this discussion, turn-on refers to either applying the power supply voltage or when the shutdown mode is deactivated. When the part is turned on, an internal current source changes the voltage of the BYPASS pin in a controlled, linear manner. Ideally, the input and outputs track the voltage applied to the BYPASS pin. The gain of the internal amplifiers remains unity until the voltage on the bypass pin reaches 1/2 V_{DD}. As soon as the voltage on the bypass pin is stable, the device becomes fully operational. Although the BYPASS pin current cannot be modified, changing the size of C_6 alters the device's turn-on time and the magnitude of "clicks and pops". Increasing the value of C_6 reduces the magnitude of turn-on pops. However, this presents a tradeoff: as the size of C_6 increases, the turn-on time increases. There is a linear relationship between the size of C_6 and the turn-on time. Here are some typical turn-on times for various values of C_6:

C_6	T_{ON}
0.01µF	30ms
0.1µF	40ms
0.22µF	60ms
0.47µF	80ms
1.0µF	140 ms

In order eliminate "clicks and pops", all capacitors must be discharged before turn-on. Rapidly switching V_{DD} on and off may not allow the capacitors to fully discharge, which may cause "clicks and pops".

AUDIO POWER AMPLIFIER DESIGN

Audio Amplifier Design: Driving 1W into an 8Ω Load

The following are the desired operational parameters:

Power Output:	$1W_{RMS}$
Load Impedance:	8Ω
Input Level:	$1V_{rms}$
Input Impedance:	20kΩ
Bandwidth:	100Hz−20kHz ± 0.25dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the Output Power vs Supply Voltage curve in the **Typical Performance Characteristics** section. Another way, using Equation (8), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the Dropout Voltage vs Supply Voltage in the **Typical Performance Characteristics** curves, must be added to the result obtained by Equation (8). The result in Equation (9).

$$V_{OUTPEAK} = \sqrt{(2R_L P_O)} \quad (8)$$

$$V_{DD} \geq (V_{OUTPEAK} + (V_{OD_{TOP}} + V_{OD_{BOT}})) \quad (9)$$

The Output Power vs Supply Voltage graph for an 8Ω load indicates a minimum supply voltage of 4.35V for a 1W output at 1% THD+N. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the HT4818/7 to produce peak output power in excess of 1.3W at 5V of V_{DD} and 1% THD+N without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the **Power Dissipation** section.

After satisfying the HT4818/7's power dissipation requirements, the minimum differential gain needed to achieve 1W dissipation in an 8Ω load is found using Equation (10).

$$A_{VD} \geq \sqrt{(P_O R_L)}/(V_{IN}) = V_{orms}/V_{inrms} \quad (10)$$

Thus, a minimum gain of 2.83 allows the HT4818/7's to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_{VD} = 3$.

The amplifier's overall gain is set using the input (R1 and R9) and feedback resistors R2 and R8. With the desired input impedance set at 20kΩ, the feedback resistor is found using Equation (11).

$$R_2/R_1 = A_{VD}/2 \quad (11)$$

The value of R_f is 30kΩ.

The last step in this design example is setting the amplifier's −3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100Hz/5 = 20Hz$$

and an

$$f_H = 20kHz*5 = 100kHz.$$

As mentioned in the **External Components** section, R_1 and C_1 create a highpass filter that sets the amplifier's lower bandpass frequency limit. Find the coupling capacitor's value using Equation (12).

$$C_1 \geqslant 1/(2\pi R_1 f_L) \quad (12)$$

The result is

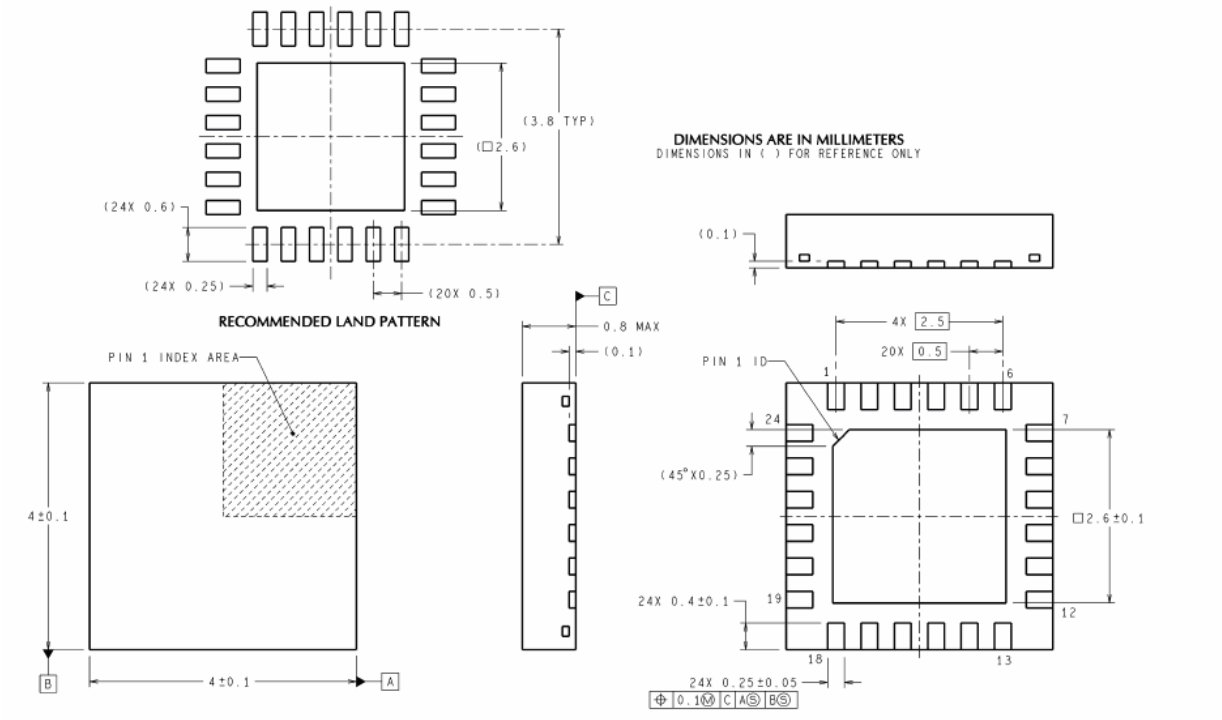
$$1/(2\pi * 20k\Omega * 20Hz) = 0.398\mu F.$$

Use a 0.39µF capacitor, the closest standard value. The product of the desired high frequency cutoff (100kHz in this example) and the differential gain, AVD, determines the upper passband response limit. With $A_{VD} = 3$ and f_H =100kHz, the closed-loop gain bandwidth product (GBWP) is 300kHz. This is less than the HT4818/7's 3.5MHz GBWP. With this margin, the amplifier can be used in designs that require more differential gain while avoiding performance-restricting bandwidth limitations.

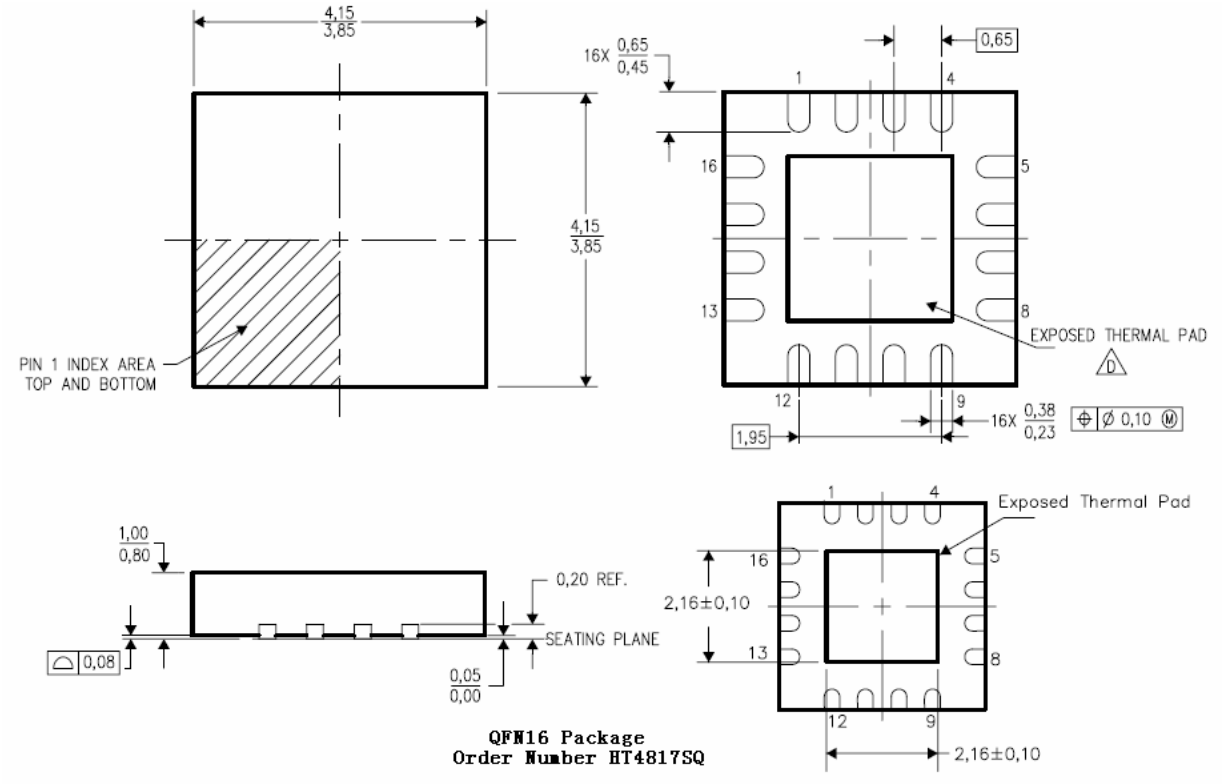
RECOMMENDED PRINTED CIRCUIT BOARD LAYOUT

Figures 3 through 6 show the recommended two-layer PC board layout that is optimized for the 24-pin SQ package. These circuits are designed for use with an external 5V supply and 8Ω, 4Ω, 3Ω speakers. These circuit boards are easy to use. Apply power and ground to the board's V_{DD} and GND pads, respectively. Connect the speakers between the board's −OUTA and +OUTA and OUTB and +OUTB pads.

Physical Dimensions inches (millimeters) unless otherwise noted



QFN24 Package
Order Number HT4818SQ



QFN16 Package
Order Number HT4817SQ